IN THE SPECIFICATION:

A) Please replace the Summary Of The Invention section with the following new text:

The present invention more specifically aims at providing an access control method which does not definitively block the access to protected memories. The present invention also aims at providing a solution which enables the integrated circuit manufacturer and/or the application program designer to individualize the access controls to the different memories. The present invention also aims at providing a solution in which it is not sufficient to have an access code or key to have access to protected memories.

According to an aspect of the invention, a method for controlling the access to all or part of the content of a first memory integrated with a microprocessor is described. The method involves executing an access control algorithm contained in a second auxiliary memory using a priority-holding interrupt (PRIORIN), then, accessing the content of the first memory with the access control algorithm using at least one register of keys. In this method, the second auxiliary memory is distinct from the first memory and the content of the auxiliary memory is programmable only once.

At least one sub-program enabling authorizing the execution of a function of accessing the first memory may be contained in the auxiliary memory. The PRIORIN is non-interruptible, even by itself. The PRIORIN is generated provided that a signal indicative of an access control operating mode is in an active state. The PRIORIN can be generated upon occurrence of an interrupt request coming from the outside of the integrated circuit or from the inside. The first memory may be a program memory containing embarked functions. The storage element may be formed by the program memory.

According to another aspect of the invention, a circuit integrating a microprocessor and at least one first memory is disclosed. The circuit includes a second

auxiliary memory adapted to contain at least one sub-program for authorizing the execution of a function of accessing the first memory. The auxiliary memory is programmable only once.

The circuit further includes means for selecting, at the input of a memory interface of the microprocessor, a memory from among at least the auxiliary memory, and the first memory. The selection of the first memory, otherwise than for the execution of a function that it contains, requiring an authorization from an algorithm contained in the auxiliary memory and using the content of at least one integrated storage element and the content of the key register. The first memory and the storage element may be one and the same program memory.

According to another aspect of the invention, the circuit further includes means for generating a PRIORIN for executing the sub-program. The PRIORIN being generated, provided that a signal indicative of an access-control operating mode is in an active state, an access to the first memory has been requested otherwise than for a non-interruptible execution of one of the functions that it contains, and an interrupt signal is active, the resulting PRIORIN being non-interruptible, even by itself.

The foregoing objects, features and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

B) Please replace the text appearing in the Detailed Description section from page 5, line 22 to page 6, line 21 with the following replacement text:

The actual microprocessor components are gathered within a block 10 shown in FIG. 1. The microprocessor components include an operator block 11 (OPE); a program counter 12 (PC); an interrupt controller 13 (INTERR CTRL); a memory interface 14 (MEM INTERF) through which transit the read and/or write addresses in memories 2, 3, and 4 and the data from and towards these memories as well as the read and write control signals; an instruction decoder 15 (DECOD); one or several internal registers 16 (INTREG); and a circuit 17 (SFR BUS INTERF) of interface with a bus (SFR BUS) intended to enable communication between

microprocessor 10 and user registers integrated in circuit 1. The operator block 11 (OPE) may include, among other things, an arithmetic and logic unit (ALU), multipliers (MULT), etc.

Circuit 1 may also integrate input/output ports 6 (I/O) which individually communicate with the outside of circuit 1. The circuit 1 may further include an external interface 7 (EXT INTERF) and standard peripherals 8 (PERIPH), for example, a serial port (UART), one or several timers (TIMER), etc.

According to an embodiment of the present invention, circuit 1 may also include an auxiliary memory 20 (AUX MEM) intended to contain sub-programs enabling the authorization (by means of algorithms) of the execution of a function to access the content of a memory to be protected and executing this function; one or several registers 21 (K REG) intended to contain access keys used by the algorithms of the auxiliary memory, these registers 21 communicating, for example, with circuit 17; a memory multiplexing circuit 22 (MEM MUX); a selector 23 (SEL) of the memory to be used; and a generator 24 of a priority-holding interrupt (PRIORIN GEN).

C) Please replace the text appearing in the Detailed Description section on page 7, lines 10 through 18 with the following replacement text:

According to another embodiment of the invention, interrupt generator 24 receives the following signals from decoder 15: an external interrupt signal EXTPRIORIN; a signal MODE, set by the user or the designer, and indicative of the desired operating mode between a normal exploitation mode of the integrated circuit and a mode of protected access to program memory 2; and an internal interrupt signal INTPRIORIN.